

Amendments to the Claims:

This listing of claims will replace all previous versions of the claims:

1. (Original) An indium phosphide-based semiconductor double hetero-structure bipolar transistor comprising: an emitter region having a first bandgap;
a base region in electrical communication with the emitter region, the base region having a second bandgap different from the first bandgap; and
a collector region containing indium and phosphorous and in electrical communication with the base and the emitter regions, the collector region having a third bandgap different from the second bandgap, the collector region containing at least three layers having different carrier concentrations.
2. (Original) The transistor as recited in claim 1, further comprising a sub-collector in electrical communication with the collector region, wherein the collector region comprises a first layer, a second layer adjacent to the first layer that has a lowest carrier concentration of the three layers, and a third layer adjacent to the second layer that has a highest carrier concentration of the three layers, and the first layer is closer to the sub-collector than either the second or third layers.
3. (Original) The transistor as recited in claim 2, wherein the second layer is an unintentionally doped layer.
4. (Original) The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the first layer to the second layer is at least about 3.
5. (Original) The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the third layer to the first layer is at least about 3.
6. (Original) The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the third layer to the second layer is at least about 10.
7. (Original) The transistor as recited in claim 2, wherein the first layer is donor doped and has a carrier concentration of about $3 \times 10^{16} \text{ cm}^{-3}$.
8. (Original) The transistor as recited in claim 2, wherein the first layer is about 500 nm thick.

9. (Original) The transistor as recited in claim 2, wherein the second layer has a carrier concentration level at most about $1\text{E}16\text{ cm}^{-3}$.

10. (Original) The transistor as recited in claim 2, wherein the second layer is about 250 nm thick.

11. (Original) The transistor as recited in claim 2, wherein the first layer has a substantially uniform carrier concentration.

12. (Original) The transistor as recited in claim 2, wherein the first layer has a graded carrier concentration that increases with increasing distance from the second layer.

13. (Original) The transistor as recited in claim 12, wherein the carrier concentration in the first layer is continuous across substantially the entirety of the first layer.

14. (Original) The transistor as recited in claim 2, wherein the collector region further comprises at least one additional layer disposed between the first layer and the sub-collector, a carrier concentration of the additional layer greater than the carrier concentration of the first layer.

15. (Original) The transistor as recited in claim 14, wherein a plurality of additional layers are disposed between the first layer and the sub-collector, carrier concentrations of the additional layers increasing with increasing distance from the first layer.

16. (Original) The transistor as recited in claim 15, wherein the carrier concentrations of the additional layers are substantially constant throughout each of the additional layers.

17. (Original) The transistor as recited in claim 15, wherein the carrier concentration of at least one of the additional layers is graded.

18. (Original) An indium phosphide-based semiconductor double heterostructure bipolar transistor comprising: an emitter region having a first bandgap;

a base region in electrical communication with the emitter region, the base region having a second bandgap different from the first bandgap; and

a collector region in electrical communication with the base and emitter regions, the collector region having a third bandgap different from the second bandgap; and

a sub-collector in electrical communication with the collector region, wherein the collector region contains indium and phosphorous, the collector region containing at least three layers having different conductivities.

19. (Original) The transistor as recited in claim 18, further comprising a sub-collector in electrical communication with the collector region, wherein the collector region comprises a first layer, a second layer adjacent to the first layer that has a lowest conductivity of the three layers, and a third layer adjacent to the second layer that has a highest conductivity of the three layers, and the first layer is closer to the sub-collector than either the second or third layers.

20. (Original) The transistor as recited in claim 19, wherein the second layer is an unintentionally doped layer.

21. (Original) The transistor as recited in claim 19, wherein the first layer is donor doped and has a carrier concentration of about $3E16\text{ cm}^{-3}$.

22. (Original) The transistor as recited in claim 19, wherein the second layer has a carrier concentration at most about $2E16\text{ cm}^{-3}$.

23. (Original) The transistor as recited in claim 19, wherein the first layer has a substantially uniform conductivity.

24. (Original) The transistor as recited in claim 19, wherein the first layer has a graded conductivity that increases with increasing distance from the second layer.

25. (Original) The transistor as recited in claim 24, wherein the conductivity in the first layer is continuous across substantially the entirety of the first layer.

26. (Original) The transistor as recited in claim 19, wherein the collector region further comprises at least one additional layer disposed between the first layer

and the sub-collector, a conductivity of the additional layer greater than the conductivity of the first layer.

27. (Original) The transistor as recited in claim 26, wherein a plurality of additional layers are disposed between the first layer and the sub-collector, conductivities of the additional layers increasing with increasing distance from the first layer.

28. (Original) The transistor as recited in claim 27, wherein the conductivities of the additional layers are substantially constant throughout each of the additional layers.

29. (Original) The transistor as recited in claim 27, wherein the conductivity of at least one of the additional layers is graded.

30-39. (Cancelled)